Abstract

A multi-stage amplifier circuit that is arranged to minimize offset related errors in a reference circuit. The first stage circuit includes an array of amplifier circuits that receive feedback signals. The outputs of the first stage amplifier circuits are coupled together to a common node. The second stage circuit is also coupled to the common node, and arranged to drive a feedback circuit to generate the feedback signals. In one example, the feedback circuit includes a band-gap core. The second stage circuit can be arranged as part of a low-drop out (LDO) regulator. Each of the amplifier circuits in the first stage can be nulled in response to null control signals from a null control logic circuit. The overall offset in the resulting reference circuit is reduced by the selective nulling of the arrayed amplifiers in the first stage circuit.

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